Claims

[c1] What is claimed is:

1.A method of dividing a semiconductor integrated circuit pattern, the pattern comprising a plurality of cells with same shape and a polygonal planar positioned between each cell, the polygonal planar comprising two parallel horizontal edges and a plurality of vertexes, the method comprising:

depicting a division line to divide the polygonal planar positioned between each cell into a plurality of unit figures, the division line beginning along a horizontal edge of the polygonal planar, and when meeting with a vertex, the division line extending a vertical line segment from the horizontal edge to another horizontal edge.

[c2] 2.The method of claim 1 wherein the unit figures comprise a triangle, rectangle, trapezoid, and parallelogram.

[c3] 3.The method of claim 1 wherein the method of dividing a semiconductor integrated circuit pattern is used to convert circuit pattern data into input graphic data of a writer, so the writer can use the input graphic data for drawing the circuit pattern on a photo mask or a substrate.

[c4] 4.A method of dividing a semiconductor integrated circuit pattern used in a data conversion system, the pattern comprising a plurality of cells with same shape and a polygonal planar positioned between each cell, the polygonal planar comprising two parallel horizontal edges and a plurality of vertexes, the method comprising:

depicting a division line to divide the polygonal planar positioned between each cell into a plurality of unit figures, the division line beginning along a horizontal edge of the polygonal planar, and when meeting with a vertex, the division line extending a vertical line segment from the horizontal edge to another horizontal edge;

wherein the data conversion system converts the divided circuit pattern into input graphic data, so a writer can use the input graphic data for drawing the circuit pattern on a workpiece.

[c5] 5.The method of claim 4 wherein the unit figures comprise a triangle, rectangle,

trapezoid, and parallelogram.

[c6] 6.The method of claim 4 wherein the workpiece comprises a photo mask or a substrate.

[c7] 7.A method of dividing a semiconductor integrated circuit pattern, the pattern comprising a plurality of cells with same shape and a polygonal planar positioned between each cell, the polygonal planar being composed of a plurality of unit figures and the unit figures being arranged sequentially and horizontally, the method comprising:
depicting a division line to divide the unit figures of the polygonal planar into at least two regions, and two adjacent unit figures being respectively divided into different regions.

[c8] 8.The method of claim 7 wherein the unit figures comprise a triangle, rectangle, trapezoid, and parallelogram.

[c9] 9.The method of claim 7 wherein the method of dividing a semiconductor integrated circuit pattern is used to convert circuit pattern data into input graphic data of a writer, so the writer can use the input graphic data for drawing the circuit pattern on a photo mask or a substrate.